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**APPLICATION
FOR
UNITED STATES
LETTERS PATENT**

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FOR: **SURGE PROTECTION CIRCUIT FOR
SEMICONDUCTOR DEVICES**

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1 TITLE OF THE INVENTION

2 **Surge Protection Circuit for Semiconductor Devices**

3 BACKGROUND OF THE INVENTION

4 Field of the Invention

5 The present invention relates to a surge protection circuit for
6 semiconductor devices, particularly suitable for use in active matrix liquid
7 crystal displays.

8 Description of the Related Art

9 Japanese Patent Publication 11-119256 discloses a surge protection
10 circuit for a TFT (thin-film transistor) array of liquid crystal display elements
11 connected to intersections of vertical and horizontal signal lines. The drains
12 of all switching transistors are respectively connected to the vertical signal
13 lines and the gates of all switching transistors are respectively connected to
14 the horizontal signal lines. The prior art surge protection circuit is composed
15 of a first array of bi-directional nonlinear circuits associated with the vertical
16 lines and a second array of bi-directional nonlinear circuits associated with
17 the horizontal lines. Each protection circuit is formed by a pair of first and
18 second thin-film transistors. In each protection circuit, the drain and gate of
19 the first transistor are connected together to a reference voltage terminal to
20 which the source of the second transistor is also connected, and the drain and
21 gate of the second transistor are connected together to the associated signal
22 line to which the source of the first transistor is also connected. The vertical
23 and horizontal signal lines are terminated at corresponding pad terminals.
24 When high-voltage static energy builds up on a pad terminal of the LCD
25 array, one of the associated transistors is turned on to provide a low-impedance

1 path for the static energy.

2 During manufacture of a protection transistor, an interlayer contact is
3 established between the drain and the gate region by forming a contact hole
4 (throughhole) in the gate insulator using a mask so that part of the gate
5 region is exposed and depositing metal in the contact hole when the drain
6 region is completed. Alternatively, a contact hole is formed after a gate and a
7 drain region and a contact hole is provided therebetween. The gate and drain
8 regions are connected through the contact hole when a transparent
9 conductive film is deposited simultaneously with the deposition of the
10 transparent conductive film for pixel electrodes.

11 Study has recently been undertaken to cut down the manufacturing
12 cost of thin film transistor arrays by reducing masking processes. Since a
13 masking process is used for establishing an interlayer contact between drain
14 and gate electrodes, this cost reduction approach cannot be applied to the
15 prior art surge protection circuit.

16 According to Japanese Patent Publication 6-18924, surge voltage is
17 discharged through a path established between drain electrodes of adjacent
18 signal lines, rather than through the gate-drain interlayer contact. This is
19 achieved by separating signal lines at intervals of a few micrometers so that
20 capacitive coupling is established between associated pad electrodes. When a
21 high-voltage static surge develops, a potential difference occurs between
22 adjacent signal lines and the surge is spark-discharged through the capacitive
23 path and all signal lines are driven to the same potential. However, since the
24 generation of a spark is necessary for discharging surge potentials, the
25 protection circuit is not reliable.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a surge protection transistor that can be fabricated with a reduced number of production steps.

The stated object is obtained by the provision of a floating-gate field effect transistor which is configured to form a low impedance path for a surge potential which builds up in a semiconductor device to be protected.

According to a first aspect of the present invention, there is provided a surge protection device comprising a gate electrode embedded in an insulator, a source electrode and a drain electrode on the insulator, the source and drain electrodes respectively forming first and second capacitances with the gate electrode, and a semiconductor island on the insulator. The semiconductor island forms a channel between the source and drain electrodes and a third capacitance with the gate electrode, the third capacitance being smaller than either of the first and second capacitances, the source and drain electrodes being adapted for connection to external circuitry for establishing a low-impedance path when the external circuitry is subjected to a surge potential.

According to a second aspect, the present invention provides a surge protection circuit comprising a plurality of surge protection devices. Each of the protection devices comprises a gate electrode embedded in an insulator, a source electrode and a drain electrode on the insulator, the source and drain electrodes respectively forming first and second capacitances with the gate electrode. A semiconductor island is formed on the insulator, the island forming a channel region between the source and drain electrodes and a third

1 capacitance with the gate electrode, the third capacitance being smaller than
2 either of the first and second capacitances.

3 The source and drain electrodes of each of the surge protection devices
4 may be respectively connected to the drain and source electrodes of adjacent
5 ones of the plurality of surge protection devices and further connected to pad
6 electrodes of external circuitry for establishing connections with the adjacent
7 surge protection devices when one of the pad electrodes is subjected to a
8 surge potential. Alternatively, the source and drain electrodes of each of the
9 surge protection devices may be connected in series to external circuitry for
10 establishing a low-impedance path to ground when the external circuitry is
11 subjected to a surge potential.

12 According to a third aspect, the present invention provides a surge
13 protection circuit for a semiconductor display device. The display device
14 includes a first plurality of pad electrodes, a plurality of vertical signal lines
15 connected respectively to the first plurality of pad electrodes, a second
16 plurality of pad electrodes, and a plurality of horizontal signal lines
17 intersecting the vertical signal lines, the horizontal signal lines being
18 connected respectively to the second plurality of pad electrodes. The surge
19 protection circuit comprises a plurality of floating-gate field effect transistors.
20 Each transistor includes a floating gate electrode, a source electrode and a
21 drain electrode, the source and drain electrodes of each of the transistors
22 being respectively connected to the drain and source electrodes of adjacent
23 ones of the plurality of floating-gate transistors and further connected to the
24 first plurality of pad electrodes for establishing connections with the adjacent
25 floating-gate transistors when one of the first plurality of pad electrodes or

1 one of the plurality of vertical signal lines is subjected to a surge potential.
2 Alternatively, the source and drain electrodes of each of the transistors are
3 respectively connected to the vertical signal lines for establishing a low-
4 impedance path to ground when one of the first plurality of pad electrodes or
5 one of the plurality of vertical signal lines is subjected to a surge potential.

6 BRIEF DESCRIPTION OF THE DRAWINGS

7 The present invention will be described in detail further with reference
8 to the following drawings, in which:

9 Fig. 1 is a top plan view of a liquid crystal display panel of a first
10 embodiment, incorporating surge protection circuits of the present invention;

11 Fig. 2 is a plan view of a surge protection transistor of the present
12 invention;

13 Fig. 3 is a cross-sectional view taken along the lines 2-2 of Fig. 2;

14 Figs. 4 to 7 are circuit diagrams of modified arrangements of the
15 floating-gate field effect transistors of the present invention.

16 DETAILED DESCRIPTION

17 In Fig. 1, an active matrix LCD display panel according to a first
18 embodiment of the present invention is illustrated. The display panel
19 comprises a first plurality of pad electrodes 10 respectively connected to
20 vertical signal lines 11 and a second plurality of pad electrodes 12
21 respectively connected to horizontal signal lines 13. Switching transistors,
22 not shown, are connected to the intersections of the vertical and horizontal
23 signal lines. Surge protection transistors 14 are floating-gate field effect
24 transistors whose source and drain electrodes are connected to adjacent
25 vertical signal lines 11 in such a manner that the drain of one transistor and

1 the source of an adjacent transistor are connected together to the same
2 vertical signal line. Since the drain electrodes of all switching transistors are
3 connected to the vertical signal lines and their gate electrodes are connected
4 to the horizontal signal lines, the vertical signal lines are also called drain bus
5 lines and the horizontal signal lines are also called gate bus lines.

6 In Figs. 2 and 3, a representative surge protection transistor 14 is
7 shown fabricated on a common glass substrate 20 on which the gate 21 of the
8 transistor is embedded in a gate insulator 22. On the gate insulator 22 is a
9 semiconductor island 23 of amorphous silicon. The source electrode 24 and
10 the drain electrode 25 of the transistor are formed on the opposite sides of the
11 island 23 so that they are separated by a channel with a length " L_{ch} ", which
12 forms a channel capacitance " C_{ch} " with the gate 21. Source 24 and the gate
13 21 overlap with each other by a length " L_{gs} " to form a gate-source
14 capacitance " C_{gs} " and the drain 25 and the gate 21 overlap with each other
15 by a length " L_{gd} " to form a gate-drain capacitance " C_{gd} ". For a gate width
16 W_g of 24 micrometers, the overlapping lengths L_{gs} and L_{gd} are equal to 24
17 micrometers and the channel length L_{ch} is 6 micrometers. Therefore, the
18 capacitances C_{gs} and C_{gd} are equal to each other and each of these
19 capacitances is much greater than the channel capacitance C_{ch} .

20 If a positive pulse charge builds up on the source 24 of a surge
21 protection transistor 14, the source electrode is driven sharply to a positive
22 potential. Since the gate electrode 21 is floated in isolation, the presence of
23 capacitances C_{gs} and C_{gd} of equal magnitude, the positive potential at the
24 source electrode 24 raises the gate 21 to some positive level. Because
25 capacitances C_{gs} and C_{gd} are much greater than channel capacitance C_{ch} ,

1 the gate potential is raised to a point that is intermediate between the source
2 and drain potentials. Under this condition, the gate potential is higher than
3 the potential at the drain 25 and hence, the floating-gate transistor 14 is
4 switched to an ON state. In a similar manner, if the source electrode 24 is
5 negatively charged, the gate electrode 21 is driven to a negative potential that
6 is intermediate between the source and drain potentials. Since the drain
7 electrode 25 is driven close to the ground potential, the floating-gate
8 transistor 14 is turned ON. Because of the symmetrical configuration of the
9 source and drain electrodes with respect to the gate, similar events occur
10 when positive or negative static charge builds up on the drain electrode 25.

11 More specifically, if capacitances C_{gs} and C_{gd} are equal to twice the
12 value of channel capacitance C_{ch} the gate potential is approximately 40
13 percent of the potential rise of the source or drain electrode. If capacitances
14 C_{gs} and C_{gd} are equal to four times the value of channel capacitance C_{ch} the
15 gate potential is approximately 44 percent of the potential rise of the source
16 or drain electrode.

17 Due to the floating-gate field effect transistor, the need to provide
18 contact holes is eliminated, simplifying the production steps. In addition, the
19 bi-directional nonlinear operating characteristic can be obtained by a single
20 floating-gate field effect transistor 14. This is advantageous for reducing the
21 amount of space to be required for protection circuitry and allowing the
22 protection circuit to be used for a high resolution display device in which the
23 interval between successive vertical signal lines (or drain bus lines) is
24 significantly small.

25 When one of the vertical signal lines 11 is charged with a surge

1 potential, the corresponding pair of floating-gate transistors 14 are switched
2 ON. As a result, the energy at the original point divides into two charge
3 packets, which propagate along the array of transistors 14 in opposite
4 directions, successively switching them into ON state with decreasing
5 potentials to allow the charge packets to escape through the associated pad
6 electrodes 10.

7 The floating-gate field effect transistors of the present invention can be
8 arranged in a number of different ways as illustrated in Figs. 4, 5, 6 and 7.

9 In Fig. 4, the vertical signal lines 11 of the display panel are
10 respectively connected to the source electrodes of floating-gate field-effect
11 transistors 15 of the present invention and their drain electrodes are
12 connected to a common shunt line 16, which is connected to the ground.
13 When a surge potential builds up on one of the vertical signal lines, the
14 corresponding surge protection transistor 15 is turned ON, allowing the
15 charge to escape to the ground. In addition to the transistors 15, the
16 transistor array of Fig. 1 may be provided as shown in Fig. 5. Static energy
17 can be distributed along the transistors 14 and discharged individually to the
18 ground by the transistors 15. The distributed discharging effect of the array
19 of transistors 14 is effectively combined with the individual ground
20 discharging effect of transistors 15 to protect the display from significantly
21 high surge potentials.

22 Fig. 6 shows a modified arrangement of the protection circuit of Fig. 1.
23 In this modification, floating-gate field effect transistors 17A and 17B are
24 additionally connected to the opposite ends of the array of transistors 14.
25 Specifically, the source-drain path of transistor 17A is connected between a

1 transfer pad electrode 10A and the left-most transistor of the array, and the
2 source-drain path of transistor 17B is connected between the right-most
3 transistor of the array and a transfer pad electrode 10B. Transfer pad
4 electrodes 10A and 10B are connected to ground. Transistors 17A and 17B
5 provide extra ground-discharge paths to protect the display device from high
6 potential charges. For significantly high potential surges, the arrangement of
7 Fig. 7 is suitable in which the transistor array of Fig. 6 is combined with the
8 array of Fig. 4.